Amendments to the Drawings:

The attached sheets of drawings includes changes to FIGs. 5, 7, 9, 11 and 13-15. These sheets, which include FIGs. 5-16, replace the original sheets including FIGs. 5-16.

Attachment: A Complete Set of 10 Drawing Sheets
Annotated Sheets Showing Changes to FIGs. 5, 7, 9, 11 and 13-15

REMARKS/ARGUMENTS

Applicant appreciates the time and courtesy extended by the Examiner to Applicant's attorney during the telephone conference of March 3, 2005 to discuss amending the application after allowance via a 312 amendment. However, references cited on a corresponding European Search Report have come to the attention of Applicant, and a Request for Continuing Application (RCE) is being filed herewith for the Examiner to consider these references.

Amendments have been made to the specification and the drawings to correct certain minor clerical errors. No new matter is being added since the corrections would be obvious to those skilled in the art from the circuit diagrams and the timing diagrams in the drawings, and the description thereof in the specification.

Claims 1-40 remain in the present application, of which claims 1, 2, 14, 21, 24, 25, 28 and 34-36 have been amended to make minor clerical/formality corrections, and not because of any reason related to patentability. As such, applicant requests that the allowance of claims 1-40 be maintained after considering the newly cited prior art references that are enclosed herewith.

In view of the above, applicant respectfully requests an early issuance of a patent with claims 1-40. If there are any remaining issues that can be addressed over the telephone, the Examiner is invited to call Applicant's attorney at the number listed below.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By _____
Jun-Young E. Jeon
Reg. No. 43,693
626/795-9900

JEJ/vdw
Enclosures: Replacement Drawings
Annotated Drawings
FRS PAS611297.1-*-03/11/05 5:58 PM

JC112 OIPE MAR 17 2005 PATENT & TRADEMARK OFFICE

FIG.5

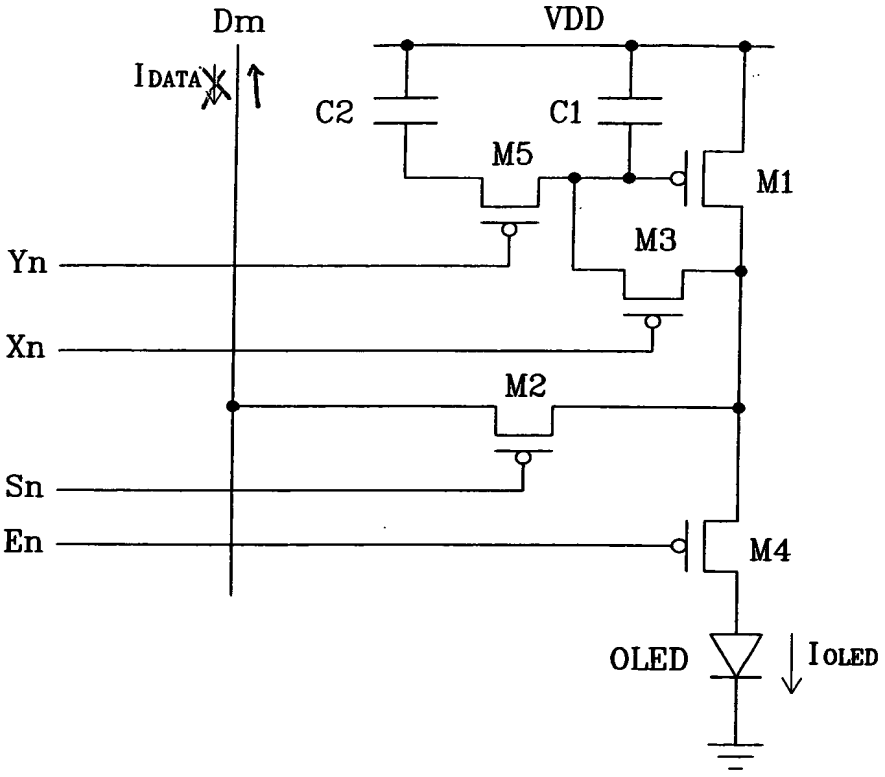


FIG.6

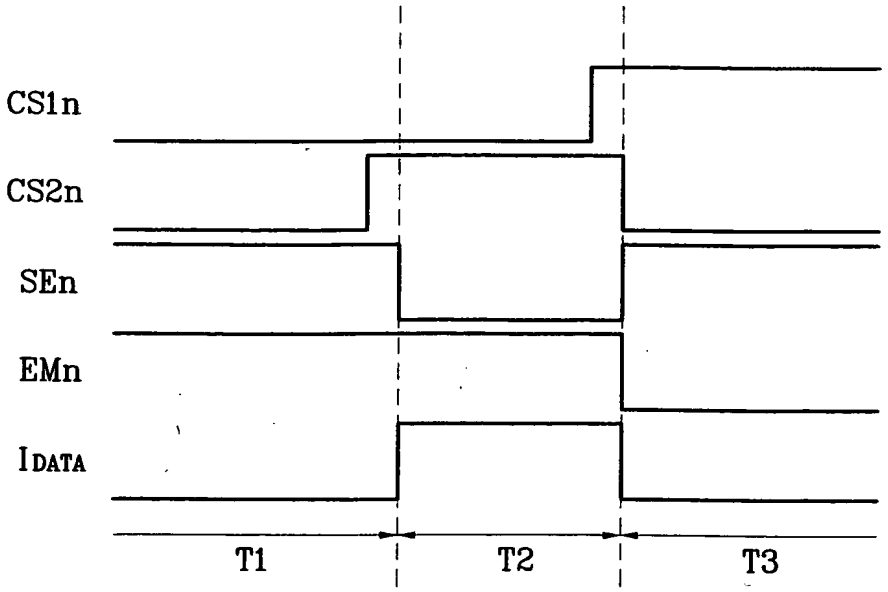


FIG. 7

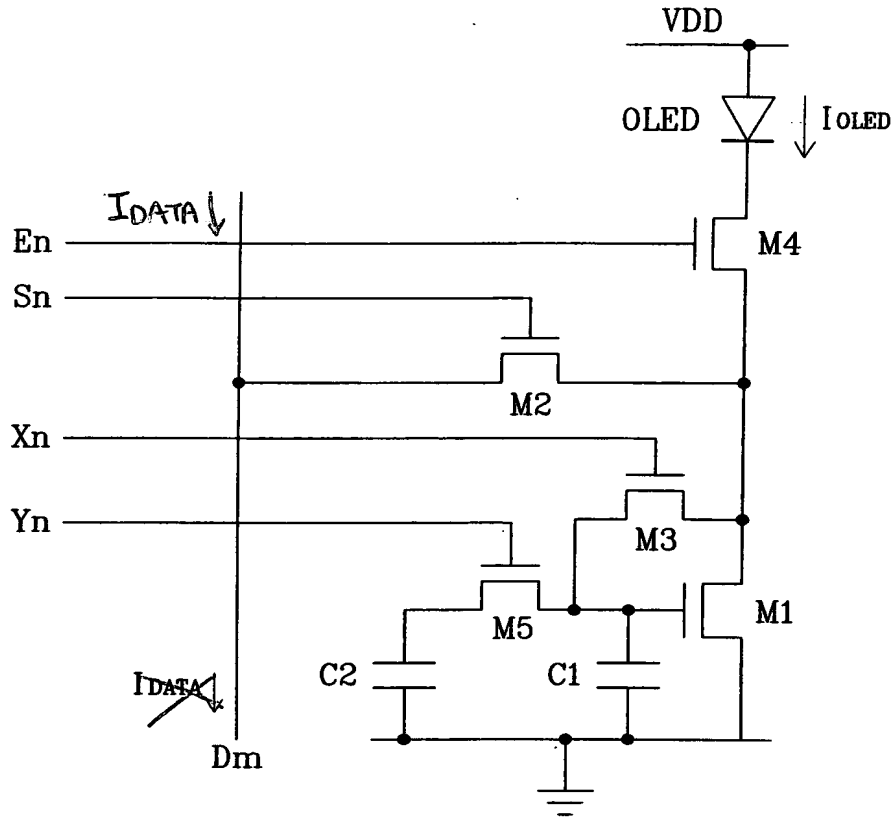

VDD
OLED
IOLED
IDATA
En
Sn
Xn
Yn
M4
M2
M3
M5
M1
C2
C1
IDATA
Dm

FIG. 8

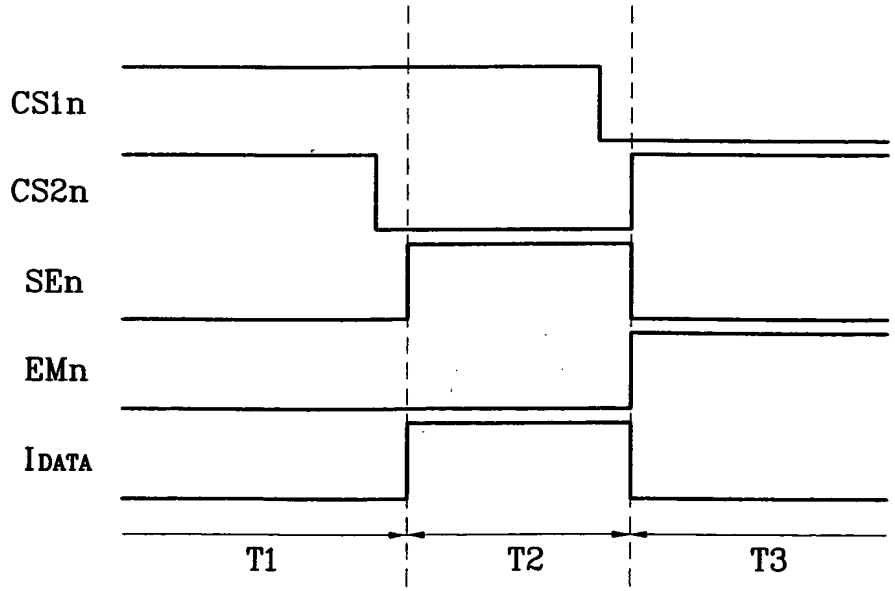

CS1n
CS2n
SEn
EMn
IDATA
T1
T2
T3

FIG. 9

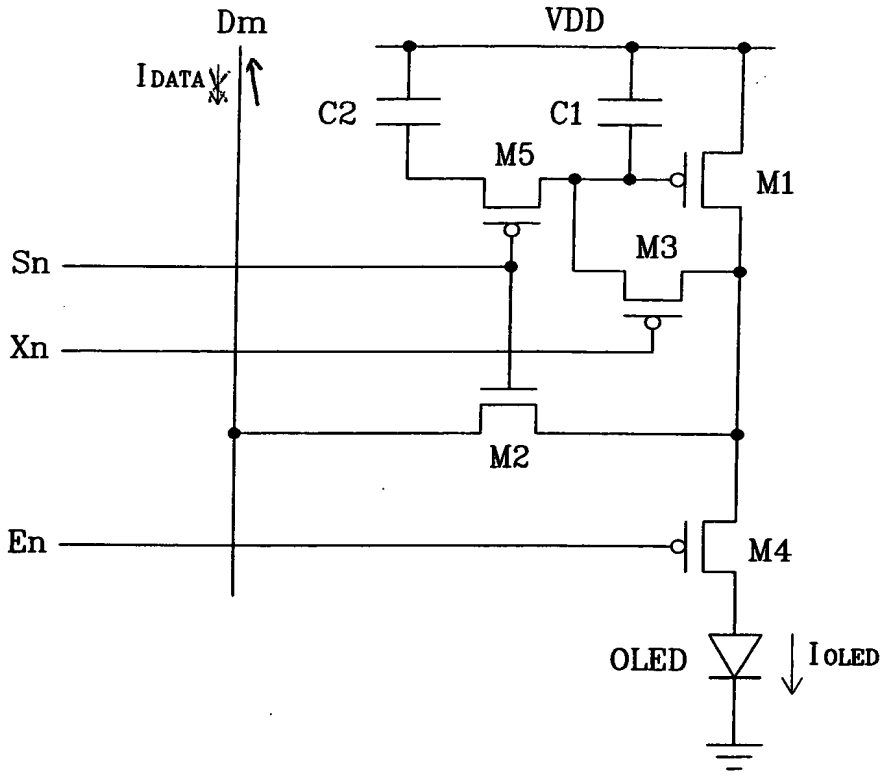

Dm
VDD
IDATA
C2
C1
M5
M1
M3
Sn
Xn
M2
En
M4
OLED
IOLED

FIG. 10

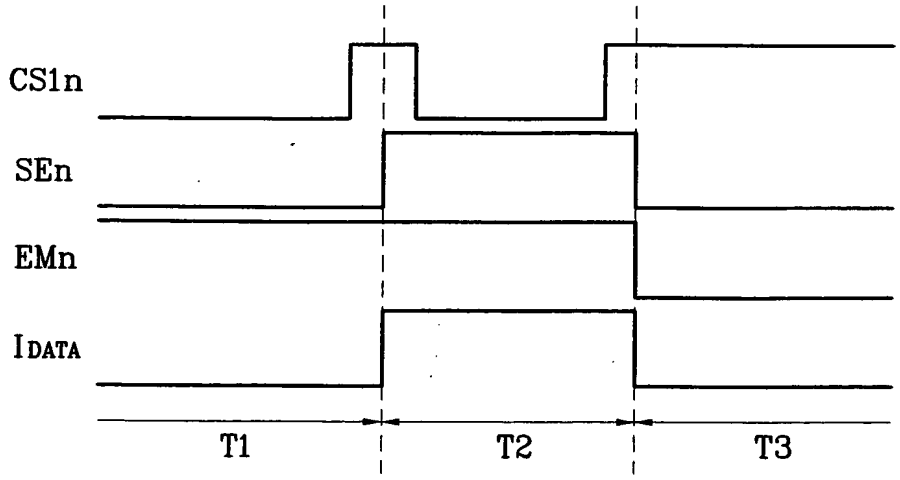

CS1n
SEn
EMn
IDATA
T1
T2
T3

FIG.11

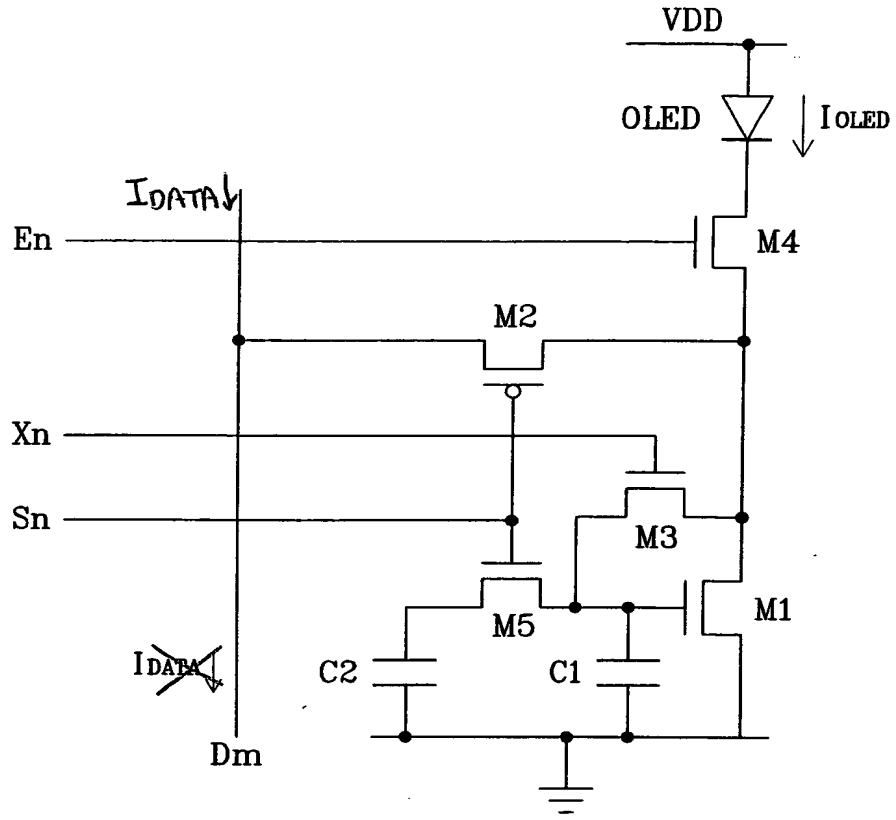

VDD
OLED
IOLED
IDATA
En
M4
M2
Xn
Sn
M3
M5
M1
IDATA
C2
C1
Dm

FIG.12

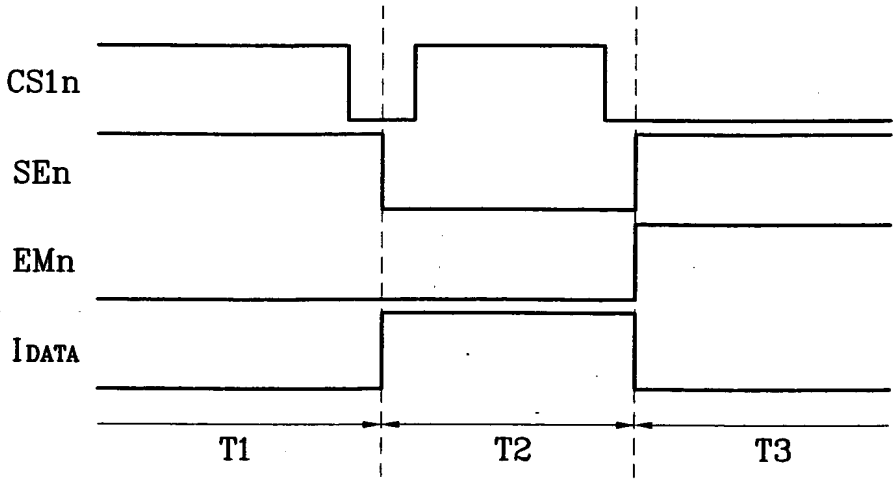

CS1n
SEn
EMn
IDATA
T1
T2
T3

FIG.13

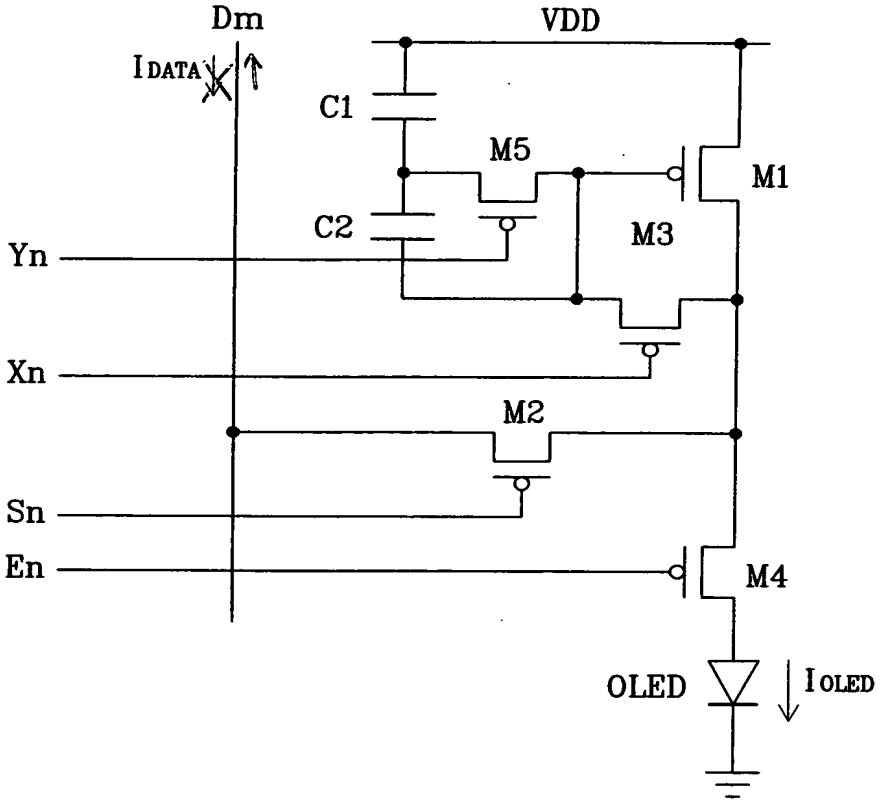


FIG.14

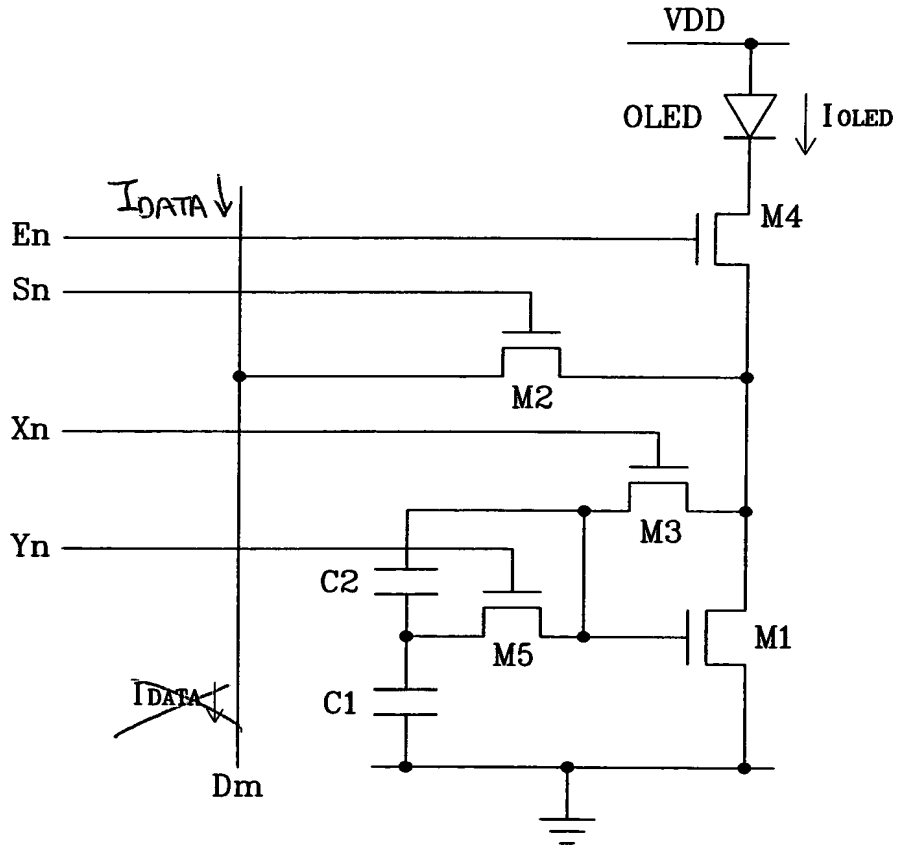


FIG.15

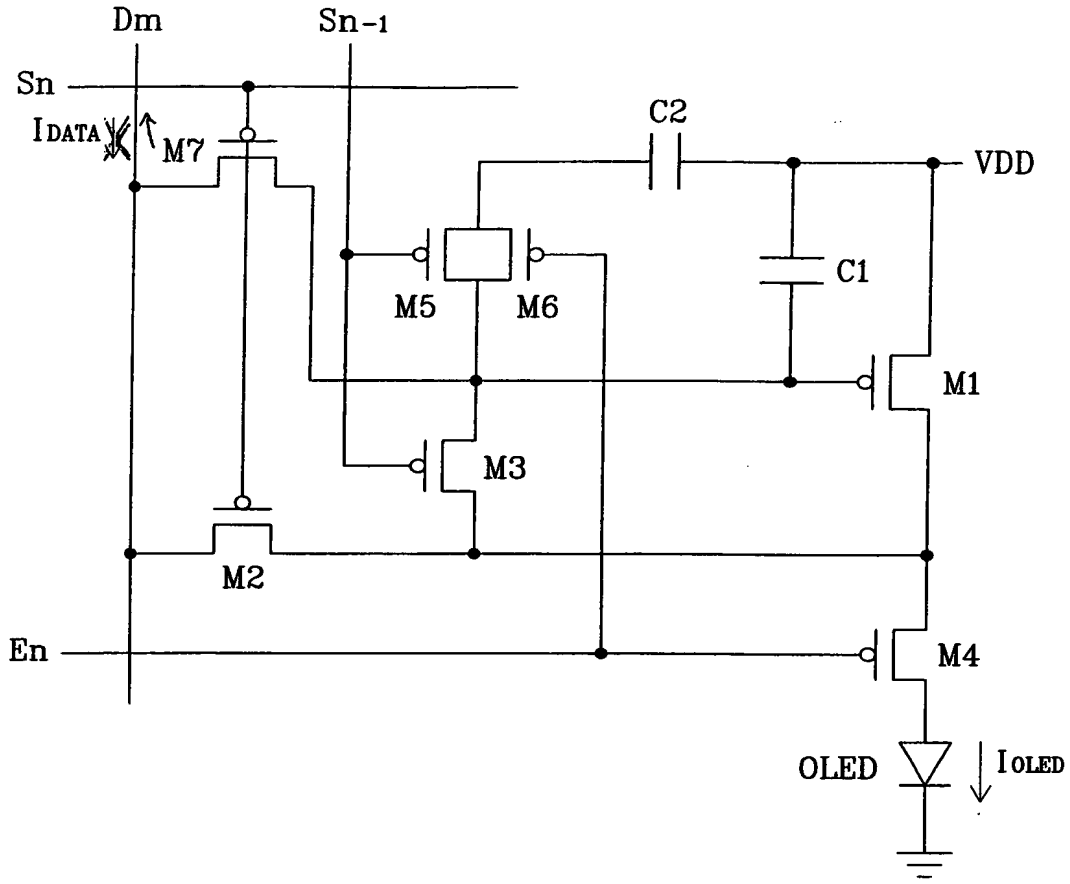
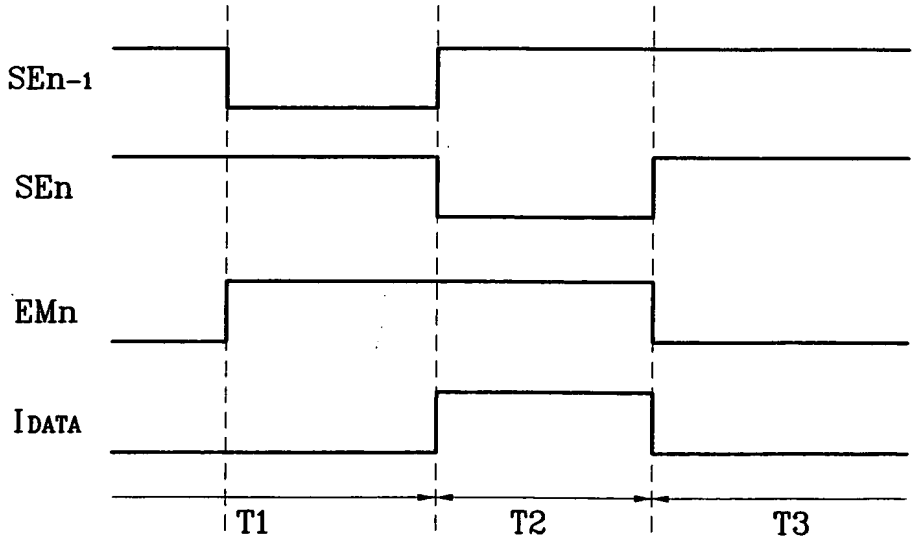

Dm
Sn-1
Sn
IDATA
M7
C2
VDD
C1
M5
M6
M1
M3
M2
En
M4
OLED
IOLED

FIG.16


SEn-1
SEn
EMn
IDATA
T1
T2
T3